Intermodulation Products - Vivace platform Specifications

2020-03-06

RF inputs

# ports	8
Impedance	50 ohm
Coupling	AC
Bandwidth	10 MHz to 4 GHz
Sampling	12 bit ADC up to 4096 MSample/s
Range	5.9 dBm (0.6 V_{peak})

RF outputs

# ports	8
Impedance	50 ohm
Coupling	AC + bias
Bandwidth	10 MHz to 4 GHz
Sampling	14 bit DAC up to 6550 MSample/s
Range	0.5 dBm (0.3 V_{peak})
Bias	Built-in bias tee for DC offset,16 bit DAC, ±1.25 V

Digital markers / triggers

# input ports	4
Input impedance	10 kohm
# output ports	4
Output impedance	50 ohm
Output voltage	3.3 V

Noise and distortion

Input voltage noise	<10 nV/sqrtHz above 1 MHz
Output-input total harmonic distortion*	-52 dBc at 100 MHz
Output-input intermodulation distortion**	- 83 dBc at 100 MHz
RF signals cross talk	- 95 dBc at 100 MHz

* THD from 2nd and 3rd harmonic ** IMD from 3rd and 5th order

Clock reference

Internal	oven-controlled crystal oscillator, ±10ppb frequency stability
External	10 MHz reference input and output

General

Size and weight	430 mm x 350 mm x 89 mm (2U, 19 inch rack)
Connectors	SMA
Communication	Gigabit Ethernet. The device is fully computer controlled (Windows, Mac and Linux compatible).
Power supply	12 V (7.5A) DC, AC/DC converter provided (100-250 V, 50-60 Hz).

Multifrequency Lockin mode

- 32 frequencies
- 32 programmable amplitudes and phases for each output port (8x32)
- 32 measured amplitudes and phases for each input port (8x32)
- Direct mode: 10 to 500 MHz
- Mixed mode: +- 250 MHz band around 0 to 4 GHz carrier (digital up- and down-conversion).

Pulse sequencer mode

- *Output, at each port (x8)*
  - 16 templates (direct output) or envelopes (multiplied by carrier)
  - Maximum template length 1 us (concatenation and continuous looping possible)
  - Template sampling resolution 250 ps
  - 1 carrier-tone generator with user-defined frequency and phase
  - 1 user-defined scaling factor
- *Input, at each port (x8)*
  - Maximum continuous-sampling window 4 us
  - Averaging of multiple windows in FPGA, maximum 100k windows at full-scale input
  - Template-matching (state discrimination) in FPGA, 16 templates
- *Experiment design*
  - Stepper with 512 values of frequency, phase and scaling factor for each output port
  - Event coordinator for timing of input and output sequences, 4096 events
  - Event time resolution 2 ns
  - Fast feedback from template matching, total latency < 200 ns