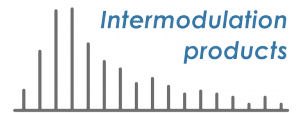


MLA – Multifrequency Lock-in Amplifier



Specifications: IMP-MLA 40-40

Lock-in

Number of frequencies	32 (40)	Can be distributed on the available input and output ports. Higher value when sampling frequency is limited to <50Msamples/s
Maximum time constant	18 – 1795 s	2 ³² samples (i.e. 18 s at 250 Msamples/s, 1795 s at 2.5 Msamples/s)
Minimum time constant	10 ns	4 samples (for continuous transfer to computer minimum 30 μs)
Data transfer rate to computer	35 000 packets/s	Each packet contains 32 (40) I-channel and 32 (40) Q-channel values
Frequency resolution	0.23 mHz – 0.22 μHz	Sampling frequency / 2 ⁴⁰
Phase resolution	0.33 nano deg	360 deg / 2 ⁴⁰

Analog ports

Port name	Max sampling frequency* [MSPS]	Bit resolution [bits]	Voltage range	Coupling	Analog bandwidth** [MHz]	Impedance*** [Ohm]
IN 1	250	14	6 Vpp	AC	50 (1250)	1346
IN 2	250	14	– 0.75 V to + 0.75 V	DC	50 (1250)	402
IN 3	62.5	16	2 Vpp	AC	25 (550)	402
IN 4	62.5	16	–1 V to +1 V	DC	25 (550)	402
OUT 1	250	16	–2 V to +2V	DC	50 (250)	50
OUT 2	250	16	–2 V to +2V	DC	50 (250)	50
OUT A	0.8	16	–4.1 V to +4.1 V	DC	0.5	50
OUT B	0.8	16	–4.1 V to +4.1 V	DC	0.5	50
OUT C	0.8	16	–4.1 V to +4.1 V	DC	0.5	50
OUT D	0.8	16	–4.1 V to +4.1 V	DC	0.5	50

* Sampling frequency is selectable to 2500 MSPS / n where 10 ≤ n ≤ 1045 is integer.

** Number in parenthesis denotes the bandwidth of the data converter which is achievable if the antialias filter is removed.

*** For optimal noise and distortion properties, the MLA exposes the bare analog AD-converter driver interface. In many cases, an application specific pre-amplifier is required. In an AFM, such pre-amplifier is usually integrated in the AFM head. If you don't have a pre-amplifier for your application, Intermodulation Products can help you choose one that is optimal for your particular application.

Clock synchronization

Port name	Default frequency	Selectable frequency	Voltage ranges	Coupling
REF CLK IN	10 MHz	100 MHz × R/N (±40 ppm) where R<16384 and N<4095 are integers	0.25 – 2.4 Vpp	AC
REF CLK OUT	10 MHz	2500 MHz/N where N<1045 is an integer	0.7 – 2 Vpp	AC

Triggers

	Number of ports	Voltage standard*	Max output current	Impedance
TRIGGER INPUT	3	2.5 V, 3.3 V or 5 V		High
TRIGGER OUTPUT	3	2.5 V, 3.3 V or 5 V	50 mA	50 Ohm

* Voltage standard is selectable with a jumper

Digital IO

Location	Number of connections	Speed	Voltage standard	Connection
High-speed connector	36 (or 18 LVDS pairs)	1 GHz	2.5 V (or LVDS)	FPGA logic
Pin header (2.54 mm)	9	5 MHz	2 x 3.3 V + 7 x 2.5 V	FPGA logic
Pin header (2.54 mm)	8	5MHz	2 x 3.3 V + 6 x 1.8 V	Processing system